is responsive to said [control] configuration data to provide different video processing operations on the video data;

[wherein] said processing module [detects the presence of] detecting each video processing module connected to said global control bus; and [passes] passing said [control] configuration data directly to each detected video processing module over said global control bus to program said parallel pipelined video hardware to perform at least one of said video processing operations.

25. (Twice Amended) The method of claim 21, wherein said [control] configuration data comprises respective control signals for each hardware component of said video processing system, the method including the step of coupling said processing module to manipulate said control signals to program said hardware components for each of said different video processing operations.

26. (Twice Amended) The method of claim 22, comprising the steps of configuring the video processing module to automatically compensate for differences in input video timing between two respective input images, including respective combinations of video data and video timing signals provided by said crosspoint switch and to provide [dual image] pointwise video processing operations using the two input images and image accumulations of said respective images.

REMARKS

Claims 1 through 30 are pending in the above identified application. Claims 1, 2, 4, 5, 6, 13, 19, 20, 25 and 26 have been amended. Basis for these amendments may be found in the specification at page 8, line 28 through page 9, line 3; at page 10, line 25 through page 11, line 5; at page 12, lines 9 - 13; at page 21, lines 25 - 29; at page 46, line 13 through page 47, line 5 and in Figures 1 and 2.

Claims 4 and 26 were rejected under 35 U.S.C. § 112. This ground for rejection is overcome by amending claims 4 and 26 to make it clear that two separate

image streams are being concurrently processed. Basis for this amendment may be found in the specification at page 12, lines 9 - 13.

Claims 1-3, 20, 21, 22, 24, 25 and 27-30 were rejected under 35 U.S.C. § 102 (e) as being anticipated by Grove et al. (hereinafter Grove). This ground for rejection is overcome by the amendments to claims 1, 20 and 25. In particular, Grove does not disclose or suggest:

> a global video bus which establishes a direct connection between the processing module and said at least one video processing module to route the video data between said processing module and said at least one video processing module; and
>
> a global control bus which provides said configuration data to/from said processing module from/to said at least one video processing module, said global control bus being separate from said global video bus

as set forth in amended claim 1,

> providing a global control bus separate from the global video bus;
>
> connecting a processing module containing at least one general purpose microprocessor to said global video bus and said global control bus said microprocessor controlling hardware and software operations of said video processing system using configuration data and processing said video data;
>
> connecting said global control bus and said global video bus to at least one video processing module which contains parallel pipelined video hardware that is responsive to said configuration data to provide different video processing operations on the video data;
>
> said processing module detecting each video processing module connected to said global control bus; and passing said configuration data directly to each detected video processing module over said global control bus to program said parallel pipelined video hardware to perform at least one of said video processing operations

as set forth in amended claim 20 or

> a general processing module containing a general purpose microprocessor which controls hardware and software operation of said

specialized processing module and said general processing module, using a hardware control library loaded on said general purpose microprocessor, said hardware control library comprising a set of functions for programming said parallel pipelined hardware of said at least one specialized processing module and said microprocessor of said general processing module to perform predetermined specialized processing operations on the input stream of data; and

a global control bus which provides control data to/from said hardware control library of said general processing module from/to said at least one specialized processing module separate from said stream of input data to be processed by said general processing module and said at least one specialized processing module.

as set forth in claim 27.

Grove discloses a crossbar switch 20 that connects a master processor, several parallel processors and a transfer processor to a group of shared memories 10. The processors can only communicate with each other through the memories 10. (See col. 11, line 66 through col. 12, line 14). In addition, Grove discloses a MIMD communication/synchronization network 40 that connects the various processors to communicate synchronization signals among the processors. (See col. 10, lines 2-5, col. 42, lines 12-24 and Col. 40, lines 23-34). Only synchronization signals are available on the bus 40. Image and graphic data and program data are transferred via the crossbar switch 20. (See Figs. 4 and 21 and col. 19, line 65 - col. 20, line 7).

Grove does not disclose or suggest transmitting any synchronization data or any control data from a hardware control library via the synchronization bus 40 or by any bus that is separate from the crossbar switch. Instead, configuration data (i.e. program instructions for the processors) are held in the memories 10 and are accessed by the processors via the crossbar switch. (See column 26, lines 23-40). The contents of the synchronization registers and the registers which hold the addresses of the other processors to which the one processor is synchronized are set from program instructions that are fetched by the processor via the crossbar switch 20. (See col. 19, line 65 - col. 20, line 7).

Because Grove does not disclose or suggest "a global video bus which establishes a direct connection between the processing module and said at least one video processing module" or a global control bus which is separate from the global video bus and "which provides said configuration data to/from said processing module

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from/to said at least one video processing module," Claims 1 and 20 can not be anticipated by Grove.

In addition, Grove does not disclose or suggest a hardware control library comprising a set of functions for programming said parallel pipelined hardware and a global control bus which provides control data from the hardware control library to the specialized processing module separate from the stream of input data to be processed by the general processing module. As set forth above, the bus 40 of Grove only makes synchronization signals available to the various processors. It does not provide programming data to the parallel processors as required by claim 27. Accordingly, claim 27 can not be anticipated by Grove.

The subject invention realizes a significant advantage by separating the configuration functions from the video data bus. Using the subject invention, image data to be used in an image processing operation may be loaded into a processing element as the element is being configured. In the Grove system, this may not be done as both program data and video data are provided by the same crossbar switch.

Claims 2 and 3 depend from claim 1; claims 21, 22, 24 and 25 depend from claim 20; and claims 28-30 depend from claim 27. Accordingly, claims 2, 3, 21, 22, 23, 24, 25 and 28-30 are not subject to rejection under 35 U.S.C. § 102(e) in view of Grove for at least the same reasons as the claims from which they depend.

In addition, with regard to claims 2 and 28, Grove does not disclose or suggest a crosspoint switch in each video processing module. The crossbar switch of Grove is external to the parallel processors. Claim 2 requires three busses, a global data bus, a global control bus and a crosspoint switch. Grove only discloses two busses and, as described, above, these two busses are not equivalent to any of the busses of the subject invention as defined by claim 2. Accordingly, claim 2 is not subject to rejection under 35 U.S.C. § 102(e) in view of Grove.

With regard to claims 3 and 24, as Grove does not disclose or suggest a crosspoint switch internal to each parallel processor, Grove can not disclose or suggest a crosspoint state machine internal to each video processing module or the step of connecting a crosspoint state machine to the crosspoint switch.

With regard to claims 21 and 28, Grove does not disclose or suggest the routing of timing signals with the video data over the global video bus. The Official

Action contends that the sync signal of Grove corresponds to the timing signal of the subject invention. Applicants respectfully disagree with this contention. The sync signal of Grove is made available to all of the parallel processors via the interrupt and poll bus 40 and is separate from the video data signal. As set forth at page 13, lines 16-22 of the subject application, Applicants gain a significant advantage by routing the timing signals with the video data. This advantage is not realized by Grove. Accordingly, claim 21 is not subject to rejection under 35 U.S.C. § 102(e) in view of Grove.

With regard to claim 29, Grove does not disclose or suggest the use of two general purpose microprocessors or of functions which coordinate concurrent multitask processing operations of the two general purpose microprocessors. Grove discloses only a single general purpose microprocessor 12. Accordingly, claim 29 is not subject to rejection under 35 U.S.C. § 102(e) in view of Grove.

Claims 4 and 26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Grove in view of Kent. Kent concerns an image processing system including a plurality of serially-connected processing elements. Kent does not provide the material that is missing from Grove. In addition, however, neither Grove nor Kent disclose or suggest apparatus which "automatically compensate[s] for differences in input video timing between respective images" as required by claims 4 and 26. The delay elements in Kent are predetermined delays or are set by the stage control units. (See col. 6, lines 7-11 and col. 10. lines 2-22). Neither of these schemes "automatically compensate[s] for differences in the input video timing between respective images" as required by claims 4 and 26. This automatic compensation is described in the specification at page 13, lines 9-22.

Because neither Grove nor Kent discloses or suggests this feature of claims 4 and 26, claims 4 and 26 are not subject to rejection under 35 U.S.C. § 103(a) in view of Grove and Kent.

Claim 5 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Grove in view of the Sensar VFE-100 brochure. The Sensar brochure was cited as disclosing pyramid processing of image data. The Sensar brochure, however, does not provide any of the material that is missing from Grove as it relates to claim 1 from which claim 5 depends. Accordingly, Claim 5 is not subject to rejection under 35 U.S.C. § 103(a) in view of Grove and the Sensar brochure. In addition, the only

motivation to combine Grove with the Sensar brochure comes from Applicants' disclosure. The type of image processing performed by Grove is fundamentally different from that performed by the Sensar VFE-100. It is well settled that the motivation to combine references can not come from Applicants' disclosure.

> To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.* (emphasis added)[1]

Accordingly, claim 5 is not subject to rejection under 35 U.S.C. § 103(a) in view of Grove and the Sensar brochure.

Claims 6-9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Grove in view of Bilbrey. Bilbrey concerns a video display system in which multiple video processing cards may be coupled together via the main computer bus 120 of a desktop computer such as an Apple MAC II. Bilbrey also discloses a video bus 150. The stated purpose of this bus is to provide both video data and control data to the video processing cards. (See column 4 lines 3-9 and column 4 line 62 through column 5, line 5). Bilbrey does not disclose any use for the main computer bus 120 or the bus connector 220. Accordingly, Bilbrey, like Grove, does not disclose or suggest the separation of video data and control data required by claim 1 of the subject invention from which claims 6-9 depend. In addition, Bilbrey, like Grove, does not disclose or suggest a crosspoint switch internal to the video processing cards as required by claim 2 from which claims 6-9 depend. Accordingly, claims 6-9 are not subject to rejection under 35 U.S.C. § 103(a) in view of Grove and Bilbrey for at least the same reasons as claim 1 from which claims 6-9 depend. The processor cards of Bilbrey are all image processing cards, there is no suggestion outside of Applicants own disclosure that these cards may be display processor cards, digitizer cards or correlator cards as required by claims 6-9. As set forth above, it is well settled that the motivation to produce the invention can not come from Applicants' own disclosure. Finally, Applicants respectfully traverse to the assertion in the Official

[1] MPEP §706.02(j)

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Action that image correlator cards as separable components of a video processing system were well known at the time of the invention. Pursuant to MPEP §2144.03, Applicants request that the Examiner cite a reference in support this position.

Claims 10 and 11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Grove in view of Bilbrey, Bruehl et al. (hereinafter Bruehl) and Purcell et al. (hereinafter Purcell). Bruehl is cited as disclosing a warper and Purcell is cited as disclosing a bilinear interpolator. Neither Bruehl nor Purcell discloses or suggests the separate video and control busses required by claim 1 nor the internal crossbar switch required by claim 2 of the subject invention from which claims 10-11 depend. Accordingly, claims 10-11 are not subject to rejection under 35 U.S.C. § 103(a) in view of Grove Bilbrey, Bruehl and Purcell. In addition, neither Bruehl nor Purcell discloses or suggests implementing a warper as a daughterboard for a video processing system. The only such suggestion comes from Applicants' own disclosure which is improperly being used against them.

Claims 12-19 and 23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Grove in view of Muramatsu. Muramatsu discloses a multiprocessor system having an offset address setting. Muramatsu does not disclose or suggest any signal processing operations being performed by the multiprocessors nor does Muramatsu disclose or suggest the separate video data and control bus structures required by claim 1 and 20 from which claims 12-19 and 23 variously depend. Accordingly, claims 12-19 and 23 are not subject to rejection under 35 U.S.C. § 103(a) in view of Grove and Mruamatsu for at least the same reasons set forth above with regard to claim 1.

In addition, with respect to claim 12, neither Grove nor Muramatsu discloses or suggests that "each microprocessor has an associated random access memory which is not shared with any other microprocessor" as required by claim 12. Even if Grove had two microprocessors, both microprocessors would be connected to the crossbar switch allowing both microprocessors to access all of the memories. In this way, the teachings of Grove conflict with those of Muramatsu which teaches having separate memories for each microprocessor and a shared memory. Without knowledge of the subject invention, it is doubtful that one of ordinary skill in the art would combine Grove and Muramatsu because Grove teaches that is desirable for all of the parallel processors to be able to access all of the memories. (See column 7, lines

11-24). Accordingly, claim 12 and claims 13-16 which depend from claim 12 are not subject to rejection under 35 U.S.C. § 103(a) in view of Grove and Muramatsu.

In response to the Examiner's request for more information Applicants enclose a product specification for the Xilinx XC4000 series of field programmable gate arrays. It is noted that, as date of this reference is May 14, 1999, it is not prior art in the above-identified patent application.

In view of the foregoing amendments and remarks, Applicants respectfully request that the Final rejection of claims 1-30 be reconsidered and withdrawn.

Respectfully Submitted,

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Kenneth N. Nigon

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